REMARKS

Claims 5, 29, 32, 34, 38, 40, 42, 44, 48, 50, 52, 56, 57, 67 are amended, no claims are canceled or added; as a result, claims 5-8 and 29-71 are now pending in this application.

§103 Rejection of the Claims

Claims 5-8 and 29-71 were rejected under 35 USC § 103(a) as being unpatentable over Katayama et al. (U.S. Patent No. 5,875,452) in view of Rosich et al. (U.S. Patent No. 5,587,964). Applicant respectfully traverses. Applicant herein incorporates all prior Responses by reference to preserve issues for appeal. The undersigned's intent to set forth brief comments to clarify the issues in this application.

The examiner allowed the parent application, Serial No. 08/886,753, which issued as U.S. Pat. No. 6,286,062. Applicant requests clarification as to how the examiner found the claim of the parent application allowable but rejects the present claims. For example claim 1 of the '062 patent follows:

> 1. A memory system comprising:
> a memory controller;
>
> a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;
>
> a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;
>
> a plurality of M memory devices wherein each memory device internally contains a data in and a data out buffer and contains a column decoder and a row decoder;
>
> a command buffer connected between the command and address bus and the plurality of memory devices, the command buffer receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of M memory devices; and
>
> a data buffer connected between the plurality of M memory devices and the

> bidirectional data bus, the data buffer receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of M memory devices for a write operation, the data buffer receiving and latching the data information from the plurality of M memory devices and driving the data information to the bidirectional data bus for a read operation, wherein the data buffer is shared by the plurality of M memory devices.

Claim 5 of the present application is essentially the same as the above claim 1 of the '062 patent except it includes the further feature of "a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:". Thus, claim 5 is narrower than claim 1 of the '062 patent yet claim 1 of the '062 patent was allowed and present claim 5 is rejected. Applicant requests clarification of this issue.

Reconsideration and allowance of claim 5 and its dependent claims 6-8 and 59-62 are requested.

With respect to claim 29, applicant submits that it is allowable as amended. Claim 29 now includes features that applicant can not find in either Katayama or Rosich. Examples of such features include, but are not limited to, latching the commands and addresses in the command buffers of each memory subsystem, wherein each of the command buffers is shared by M of the plurality of memory device of each memory subsystem and is positioned between the command the command and address bus and the plurality of M memory devices of each memory subsystem. To establish a prima facie case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. M.P.E.P. 2142 (citing In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)). Applicant submits that claim 29 and its dependent claims 30-31 are allowable as all of the claim features are not found in Katayama and Rosich. Reconsideration and allowance of claims 29-31 are requested.

Claim 32 recites, in part, "latching the commands and addresses in the plurality of command buffers, wherein each of the plurality of command buffers is shared by M of the plurality of memory devices and is positioned between the command and address bus and the plurality of memory devices". Applicant can not find these features in Katayama or Rosich. Accordingly, applicant submits that claim 32 and dependent claim 33 are allowable.

Claim 34 is believed to be allowable for at least substantially similar reasons as stated above with regard to claim 1. Claims 35-37 and 64 are believed to be allowable at least because they depend from claim 34.

Claim 38 is believed to be allowable for at least substantially similar reasons as stated above with regard to claims 1 and 29. Claim 39 is believed to be allowable at least because it depends from claim 38. Moreover, applicant can not find where Katayama or Rosich teach "executing a *packet protocol* which incorporates a *first delay* introduced by the command buffer and a *second delay* introduced by the data buffer" [italics added], as recited in claim 39. Reconsideration and allowance of claims 38-39 are requested.

Claim 40 recites, in part, "wherein each memory device *internally* includes a data in and a data out buffer, a column decoder and a row decoder, . . . latching the commands and addresses read from the unidirectional command and address bus in the command buffers of the plurality of memory subsystems, wherein *each of the command buffers is shared by the plurality of memory device of each memory subsystem and is positioned between the command the command and address bus and the plurality of memory devices of each memory subsystem.* Applicant can not find these features in Katayama or Rosich. As these two cited documents do not teach all of the features of claim 40, applicant requests allowance of claim 40.

Claim 41 is believed to be allowable at least because it depends from claim 40. Moreover, applicant can not find where Katayama or Rosich teach "executing a *packet protocol* which incorporates a *first delay* introduced by the command buffer and a *second delay* introduced by the data buffer" [italics added], as recited in claim 41. Reconsideration and allowance of claim 41 are requested.

Claim 42 is believed to be allowable for at least substantially similar reasons as stated above with regard to claim 40. Claim 43 is believed to be allowable at least because it depends

from claim 42. Moreover, applicant can not find where Katayama or Rosich teach "executing a *packet protocol* which incorporates a *first delay* introduced by the command buffer and a *second delay* introduced by the data buffer" [italics added], as recited in claim 43. Reconsideration and allowance of claims 42 and 43 are requested.

Claim 44 recites, in part, "wherein each memory device *internally* contains a data in and a data out buffer, a column decoder and a row decoder". Applicant can not find this feature in combination with the other features of claim 44 in either Katayama or Rosich. Reconsideration and allowance of claim 44 and claims 45-47 and 65 depending from claim 44 are requested.

Claim 48 recites, in part, "wherein each memory device *internally* contains a data in and a data out buffer, a column decoder and a row decoder". Applicant can not find this feature in combination with the other features of claim 48 in either Katayama or Rosich. Reconsideration and allowance of claim 48 and claim 49 depending from claim 48 are requested.

Claim 50 recites, in part, "wherein each memory device *includes* addressable storage, a data in and a data out buffer, a column decoder and a row decoder". Applicant can not find this feature in Katayama or Rosich. Reconsideration and allowance of claim 50 and claim 51 depending from claim 50 are requested.

Claim 52 recites, in part, "wherein each memory device *internally* contains a data in and a data out buffer, a column decoder and a row decoder". Applicant can not find this feature in combination with the other features of claim 52 in either Katayama or Rosich. Reconsideration and allowance of claim 52 and claims 53-55 and 65 depending from claim 52 are requested.

Claim 56 recites, in part, issuing commands and addresses on a unidirectional command and address bus to a plurality of memory subsystems; latching the commands and addresses in a command buffer in each of the plurality of memory subsystems; driving the latched commands and addresses to column and row decoders in each of the plurality of subsystems; retrieving data from addressable storage of only one of the plurality of memory subsystems. Applicant can not find where Katayama or Rosich teach these features. Specifically, applicant can not find where Katayama or Rosich teach issuing and latching to a plurality of memory subsystems but retrieving data from only one of the memory subsystems. Reconsideration and allowance of claim 56 are requested.

Claim 57 recites, in part, a plurality N of pipelined memory subsystems, wherein each memory subsystem includes: a plurality M of memory devices wherein each memory device *internally consists of* a data in and a data out buffer, a decoder and an array of memory cells. Applicant can not find where Katayama or Rosich teach these features. Reconsideration and allowance of claim 57 and claim 58 depending from claim 57 are requested.

Claim 62 includes the features of claim 5. Applicant submits that claim 62 is allowable for at least substantially similar reasons as stated above with regard to claim 5.

Claim 67 recites, in part, "a plurality N of pipelined memory subsystems, wherein each memory subsystem includes: a plurality M of memory devices, wherein each memory device *internally* contains a data in and a data out buffer, a column decoder and a row decoder . . ." Applicant can not find where Katayama or Rosich teach these features. Reconsideration and allowance of claim 67 and claims 68-71 depending from claim 67 are requested.

Double Patenting Rejection

Claims 5-8 and 29-71 were rejected under the judicially created doctrine of double patenting over claims 1-4, 26-28, and 32-57 of U.S. Patent No. 6,286,062. Applicant will consider filing a Terminal Disclaimer to overcome this rejection once the pending claims are in an allowable form.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box DAC, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313, on this 15 day of July, 2003.

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